METHOD OF FABRICATING CIRCULAR OR ANGULAR SPIRAL MIM CAPACITORS

FIELD OF THE INVENTION

The present invention relates generally to fabrication of semiconductor devices, and more specifically to methods of fabricating metal-insulator-metal (MIM) capacitors.

BACKGROUND OF THE INVENTION

Circular or angular spiral metal-insulator-metal (MIM) capacitors are useful semiconductor devices.

U.S. Patent No. 6,309,922 B1 to Liu et al. describes a spiral inductor process.

U.S. Patent No. 6,274,502 B1 to Ohkuni describes a circular inductor process.

U.S. Patent No. 6,258,652 B1 to Stacey describes a spiral inductor process having air gaps.

U.S. Patent No. 6,054,329 to Burghartz et al. describes another spiral inductor process.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide improved methods of forming a circular or angular spiral metal-insulator-metal (MIM) capacitors.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, substrate having a lower low-k dielectric layer formed thereover is provided with the lower low-k dielectric layer having a dielectric constant of less than about 3.0. Metal vertical electrode plates are formed within the lower low-k dielectric layer so that the adjacent metal vertical electrode plates have lower low-k dielectric layer portions therebetween. The lower low-k dielectric layer portions between the adjacent metal vertical electrode plates are replaced with high-k dielectric material trench portions having a dielectric constant of greater than about 3.0.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Fig. 1 is a top down plan view of an angular spiral MIM capacitor made in accordance with the present invention.

Fig. 2 is a top down plan view of a circular MIM capacitor made in accordance with the present invention.

Figs. 3 to 9 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention with Fig. 9 being the cross-sectional view along line 9 - 9 of Fig. 1 or line 9 - 9 of Fig. 2.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

For the purposes of this invention, a low-k dielectric material has a dielectric constant of less than about 3.0 and a high-k dielectric material has a dielectric constant of preferably greater than about 3.0 and more preferably from about 7.0 to 50.0.

Fig. 1 is a top down, plan view of an angular spiral MIM capacitor 10' made in accordance with the present invention. Spiral MIM capacitor 10' includes a spiral metal portion 12' with high-k dielectric material 14' between adjacent portions 16', 18', 20', 22', 24', 26' as shown along line 9 - 9, for example. Spiral MIM capacitor 10' is surrounded by a low-k dielectric material 30'. Fig. 1 also illustrates another metal structure 32' proximate the angular spiral MIM capacitor 10'.

Fig. 2 is a top down, plan view of a circular MIM capacitor 10" made in accordance with the present invention. Circular MIM capacitor 10" includes a circular metal portion 12" with high-k dielectric material 14" between adjacent portions 16", 18", 20", 22", 24", 26" as shown along line 9 - 9, for example. Spiral MIM capacitor 10" is surrounded by a low-k dielectric material 30". Fig. 2 also illustrates another metal structure 32" proximate the circular MIM capacitor 10".

Regardless of whether an angular spiral MIM capacitor 10' or a circular MIM capacitor 10" is to be formed, the following description of the method of the present invention applies to the fabrication of each MIM capacitor 10', 10".

For ease of understanding, the corresponding structures of angular spiral MIM capacitor 10' and circular MIM capacitor 10" will be illustrated without a prime suffix. That is, e.g., angular spiral MIM capacitor 10' and circular MIM capacitor 10" will both be annotated as MIM capacitor 10.

Figs. 3 to 9 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention with Fig. 9 being the cross-sectional view along line 9 - 9 of Fig. 1 or line 9 - 9 of Fig. 2.

It is noted that while six adjacent portions 16', 18', 20', 22', 24', 26' for a spiral MIM capacitor 10' and six adjacent portions 16", 18", 20", 22", 24", 26" for a circular MIM capacitor 10" are shown being formed in Figs. 3 to 9, one skilled in the art recognizes that less or more such respective adjacent portions may be formed depending upon the final spiral MIM capacitor 10' or circular MIM capacitor 10" desired to be fabricated.

Initial Structure - Fig. 3

Fig. 3 illustrates a cross-sectional view of a structure 40 having a low-k dielectric material layer 30 formed thereover to a thickness of preferably from about 2000 to 50,000Å and more preferably from about 5000 to 10,000Å.

Structure 40 is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers

and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

Low-k dielectric material layer 30 is preferably comprised of TEOS, FTEOS, Coral™, Black Diamond™ or an organic material and is more preferably comprised of an organic material.

A first patterned mask layer 42 is formed over the low-k dielectric material layer 30 to define the capacitor 10 vertical electrode plates 16, 18, 20, 22, 24, 26.

Formation of Vertical Electrode Plate Openings 17, 19, 21, 23, 25, 27 - Fig. 4

As shown in Fig. 4, the low-k dielectric material layer 30 is patterned using the first patterned mask layer 42 to form vertical electrode plate openings/trenches 17, 19, 21, 23, 25, 27. Trenches 17, 19, 21, 23, 25, 27 have a width of preferably from about 100 to 50,000Å and more preferably from about 5,000 to 10,000Å. (As noted above, trenches 17, 19, 21, 23, 25, 27 may comprise trenches for an angular spiral MIM capacitor 10' or a circular MIM capacitor 10".)

Trenches 17, 19, 21, 23, 25, 27 are preferably formed concomitantly with logic metal vias or trenches. For example, another opening 29 proximate the to

be formed capacitor 10 may also be formed concomitantly with trenches 17, 19, 21, 23, 25, 27 as shown in Fig. 4. It is noted that opening 29 and the metal trench structure 28 formed therein is optional.

Formation of Metal Vertical Electrode Plates 16, 18, 20, 22, 24, 26 And Metal Trench Structure 28 - Fig. 5

As shown in Fig. 5, the first patterned mask layer 42 is removed from the structure of Fig. 4 and the structure may be cleaned as necessary.

Trenches 17, 19, 21, 23, 25, 27 and proximate trench 29 are preferably lined with respective metal barrier layers 50, 52, 54, 56, 58, 60, 62 and are filled with respective planarized metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 and metal trench structure 28.

Metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 and proximate metal structure 28 are preferably comprised of copper (Cu) or tungsten (W) and are more preferably copper (Cu). Metal barrier layers 50, 52, 54, 56, 58, 60, 62 are preferably comprised of Ta or TaN and are more preferably Ta/TaN.

A second patterned mask layer 70 is then formed over patterned low-k dielectric material layer 30 to leave the portions of patterned low-k dielectric material layer 30 between the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 exposed as shown in Fig. 5.

Removal of the Exposed Patterned Low-k Dielectric Material Layer 30 - Fig. 6

As shown in Fig. 6, using the second patterned mask layer 70 as a mask, the exposed portions of patterned low-k dielectric material layer 30 between the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 are removed, preferably by etching, to form openings/trenches 72, 74, 76, 78, 80 between the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26.

Formation of High-k Dielectric Material Portions 90, 92, 94, 96, 98 - Fig. 7

As shown in Fig. 7, second patterned mask layer 70 is removed and the structure is cleaned as necessary.

Openings/trenches 72, 74, 76, 78, 80 between the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 are filled with a high-k dielectric material to form respective high-k dielectric material portions 90, 92, 94, 96, 98 between the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26. The high-k dielectric material portions 90, 92, 94, 96, 98 are preferably comprised of SiN, Ta_xO_y, Hf_xO_y, Ti_xO_y, Al_2O_3, $Ta_xAl_yO_z$, $Ti_xAl_yO_z$, SiO_2, $Ta_xN_yO_z$, $Ti_xN_yO_z$ or other non-conductive oxidized refractory metals and is more preferably a low leakage and high breakdown material.

The high-k dielectric material portions 90, 92, 94, 96, 98 are comprised of a material having a dielectric constant of preferably greater than about 3.0 and more preferably from about 7.0 to 50.0.

Formation of Optional Etch Stop Layer 100 - Fig. 7

As shown in Fig. 7, an optional etch stop layer 100 is then formed over the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26, the high-k dielectric material portions 90, 92, 94, 96, 98 therebetween and the remaining low-k dielectric material 30 as shown in Fig. 7. Optional etch stop layer 100 has a thickness of preferably from about 100 to 1000Å and more preferably from about300 to 600Å, and is preferably comprised of SiN or $Si_xO_yN_z$ and is more preferably SiN.

Formation of Upper Low-k Dielectric Material Layer 102 - Fig. 7

Then, as shown in Fig. 7, an upper low-k dielectric material layer 102 may be formed over the optional etch stop layer 100 (or over the metal vertical electrode plate structures 16, 18, 20, 22, 24, 26, the high-k dielectric material portions 90, 92, 94, 96, 98 therebetween and the remaining low-k dielectric material 30 if the optional etch stop layer 100 is not used) to a thickness of preferably from about 2000 to 50,000Å and more preferably form about 5000 to 10,000Å. The upper low-k dielectric material layer 102 is preferably comprised of TEOS, FTEOS, Coral™, Black Diamond™ or an organic material. The upper low-k layer 102 may be comprised of

the same material as the low-k layer/layer portions 30 and it is preferred that the low-k layers 30 and 102 be comprised of the same material.

A third patterned mask layer 104 is then formed over the upper low-k layer 102 with respective openings 105, 107, 109, 111, 113, 115 positioned over at least a portion of the respective metal vertical electrode plate structures 16, 18, 20, 22, 24, 26 and exposing respective portions of the upper low-k layer 102. Third patterned mask layer 104 may also include an opening or openings 121 positioned over at least a portion of the metal trench structure 28 adjacent the MIM capacitor 10 and exposing respective portion(s) of the upper low-k layer 102.

Formation of Via Openings 125, 127, 129, 131, 133, 135, 141 - Fig. 8

As shown in Fig. 8, the upper low-k dielectric layer 102 is patterned to form respective via openings 125, 127, 129, 131, 133, 135, 141 exposing respective portions of the vertical electrode plate structures 16, 18, 20, 22, 24, 26 and metal trench structure 28. If optional etch stop layer 100 is used, the patterning of the upper low-k dielectric layer 102 exposes portions of the etch stop layer 100 and then the etch stop layer 102 is patterned to expose the respective portions of the vertical electrode plate structures 16, 18, 20, 22, 24, 26 and metal trench structure 28.

Formation of Via Structures 146, 148, 150, 152, 154, 156 And Metal Via Structure 162 - Fig. 9

Via openings 125, 127, 129, 131, 133, 135, 141 may then be lined with respective via barrier layers (not shown) and then filled with respective via structures 146, 148, 150, 152, 154, 156 and metal via structure 162.

The via barrier layers are preferably comprised of Ta or TaN.

The via structures 146, 148, 150, 152, 154, 156 and metal via structure 162 are preferably comprised of copper (Cu) or tungsten (W) and are more preferably copper (Cu).

Advantages of the Invention

The advantages of one or more embodiments of the present invention include:

1) there is no sharp corners at the trench bottom leading to poor breakdown;

2) no metal etch is required so no cleaning step for a metal etch is required;

3) no topology induced due to the MIM capacitor so no oxide CMP is needed;

4) great flexibility to choices of low-k and high-k materials as there is no concern of Cu oxidation due to the high or low-k oxide material definition; and

5) simple process and structural design.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.